A New, Versatile, High-performance Digital Pulse Processor with Application to Neutron/Gamma-Ray Pulse-Shape Discrimination in Scintillator Detectors

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Abstract–

We present a VME based, 16-channel digital pulse processing module which has been developed to be suitable for a wide range of radiation detectors and to deliver high resolution in energy and time measurement. This module delivers high performance and flexibility with ease of use. A unique concept for the online digital pulse processing firmware has been developed to combine the capabilities of digitizing data acquisition with the logic to emulate the accuracy of classic analog techniques. For use with scintillating neutron detectors, the on-board firmware includes pulse-shape discrimination (PSD) in order to allow "on the fly" neutron-gamma discrimination. Since particle identification is done on board, rates up to 1 MHz are possible. Measurements with a xylene-based EJ-301 liquid scintillator, a 4"x2" Inrad Optics Stilbene crystal scintillator, as well as a 3"x3" CLYC detector will be presented. The results will be compared with data derived from analog PSD techniques.

1. MDPP-16 Digital Pulse Processor

1.1 Hardware Concept

The Mesytec MDPP-16 is a fast high-resolution time and amplitude digitizer. Figure 1 shows the module and block diagram. It is internally realized as a 16-channel adjustable low-noise amplifier and a variable-differentiation stage, followed by filters and 80 MHz sampling ADCs. The digitized data are analyzed in an FPGA and reconstructed with highest precision. This achieves unique timing (65ps) and amplitude (15bit) resolution. The MDPP-16 is capable of directly accepting any pre-amplifier or detector signal for a wide range of radiation detectors (HPGE, Si, scintillators, etc.).
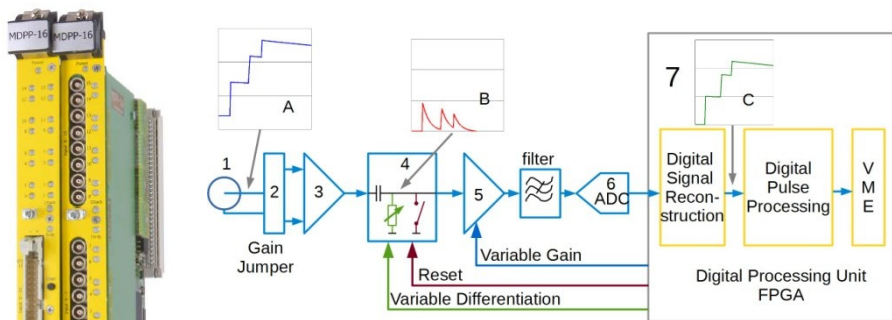
MDPP Block Diagram:
1: Input Connector: Differential or unipolar
2: Input / gain jumper: Polarity and coarse gain
3: Low Noise Amplifier: High dynamic range
4: Differentiation stage: Variable with fast reset circuit
5: Variable gain stage: 1 to 24, total continuous gain 1 to 200
6: Sampling ADC (80MHz)
7: FPGA with Digital Pulse Processing: Up to 4 different FW modules

Figure two front-panel input **configurations and** MDPP Block Diagram

To achieve a high dynamic range and allow use with various types of detectors and pre-amplifiers the MDPP-16 is outfitted with a sophisticated low-noise input stage. First, for a group of 4 channels, the input gain jumper block selects the maximum input voltage coarse range from about 300mV to some 10V, defines the input type being either differential or unipolar and sets the input termination resistance (50Ω, 96Ω or high ohmic) as well as polarity. This pre-adjustment is followed by a low noise amplifier with high dynamic range and a variable gain amplifier with gain settings between 1 and 24. Adding a software gain of another factor of 10, the user can set the gain from 1 to 250 in steps of 1%. The resulting lowest range with 300mV gain jumpers and gain = 24 is about 12 mV (excluding the software gain).
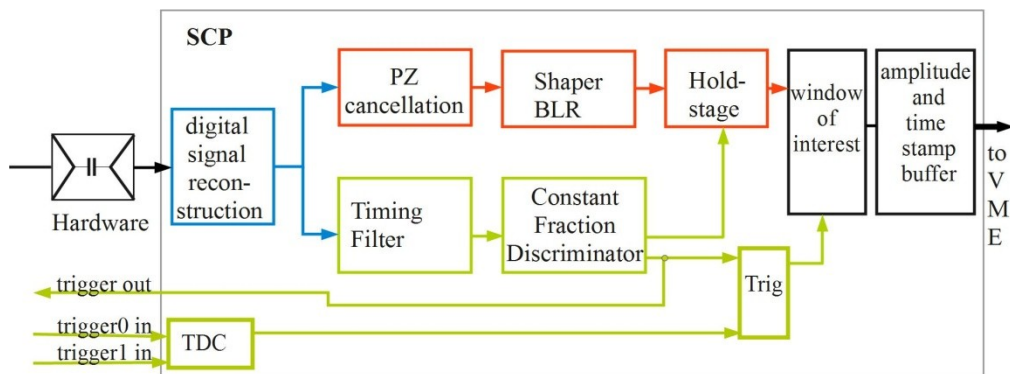
When digitizing charge integrating preamplifier signals at high rates, pile-up becomes a limiting factor for the available dynamic range. That is due to the long decay times of the integrated signals and resulting stacking of pulses on the tails of preceding pulses. To avoid excessive clipping, the input range has to be adjusted to accept several times the maximum signal amplitude.

To overcome this, and also to make the MDPP-16 insensitive to DC-offsets, a pre-differentiation is implemented in the low-noise input section. The pre-differentiation is internally adjusted in dependence of the shaping time settings in the digital pulse processing. This guarantees that in all reasonable operation conditions, pile-up stacking and offsets can be neglected and the full dynamic range of the ADC is available.

1.2 SCP Firmware

The standard SCP firmware, designed to process signals from charge integrating pre-amplifiers, is separated in an energy path with high-quality trapezoidal shaping from 50 ns to 25 us (FWHM), a PZ adjustment from 800ns to infinity, and a high-performance self-adjusting Baseline restorer. Figure 2 shows the SCP Firmware block diagram.

The digital pulse processing firmware in the FPGA follows the classic analog processing path while using the precision of digital filters. The achieved energy resolution is 15 bit (32k) for a shaping time of 2us. For timing, the digital reconstructed signal is going through an independent trapezoidal timing filter amplifier (TFA) with down to 15ns integration time. The signal is then processed by a Constant Fraction Discriminator (CFD) with a fraction of 50%, providing 65 ps RMS timing resolution between two channels. The resolution of timing difference is independent of the signal delays between two inputs.

Figure 2 SCP Firmware to process signals of a Standard Charge Integrating Preamplifier

The digitization frequency of 80 MHz is sufficient to analyze signals with 15 ns rise time without loss of information and results in timing and amplitude resolution being very close to ideal.

MDPP-16 requires just a few essential parameters to be defined for the digitization and processing. The coarse gain and polarity is set by gain jumpers. Another factor of 200 in gain can be set by a single parameter, which

controls hardware and software gain to minimize noise. The signal rise time is used for ballistic loss correction especially with large coaxial germanium detectors and determines the flat top of trapezoidal shaping curve. For pulse processing and analysis only the shaping time (width of triangular shaping), the timing filter time constant and the trigger threshold have to be defined. All needed internal settings and parameters are internally calculated from those primary ones. Two monitoring outputs allow the user to see the digitally reconstructed signals on an oscilloscope, and optimize the above settings for each channel. It also helps to debug the signal chain from detector to digitization.

1.3 RCP Firmware

Reset amplifiers provide the lowest thermal noise of all charge integrating preamplifiers. The input charge is integrated to a step. When the accumulated steps reach the maximum output voltage, a reset sets the baseline back to the minimum voltage. It is mainly used to amplify signals of HPGe detectors which detect energies in the keV range, but also for higher energies in the MeV range. The reset step may be 2 V for example, while the signal is only 35 mV/MeV. This results in an input range to noise ratio of 3×10^5, which usually exceeds the signal to noise ratio of any straight-forward sampler. Figure 3 shows the RCP Firmware block diagram.

To meet this challenge, the accumulated offset of the signal is eliminated by the pre-differentiation. When a reset pulse is detected, which can be 100 times larger than the detector signals, the pre-differentiation time constant is reduced to about 100 ns. This allows suppression of the reset pulse within 2 µs. The reset stage allows a theoretical reset time of about 2 µs, but usually the RESET preamplifiers need some 10 µs to fully recover by themselves. Thus a definable time can be configured to disable the signal processing during that time. To handle signals from RESET type preamplifiers, the RCP Firmware has an additional reset-controller implemented which manages the reset timing, and resets the hardware and digital filters.
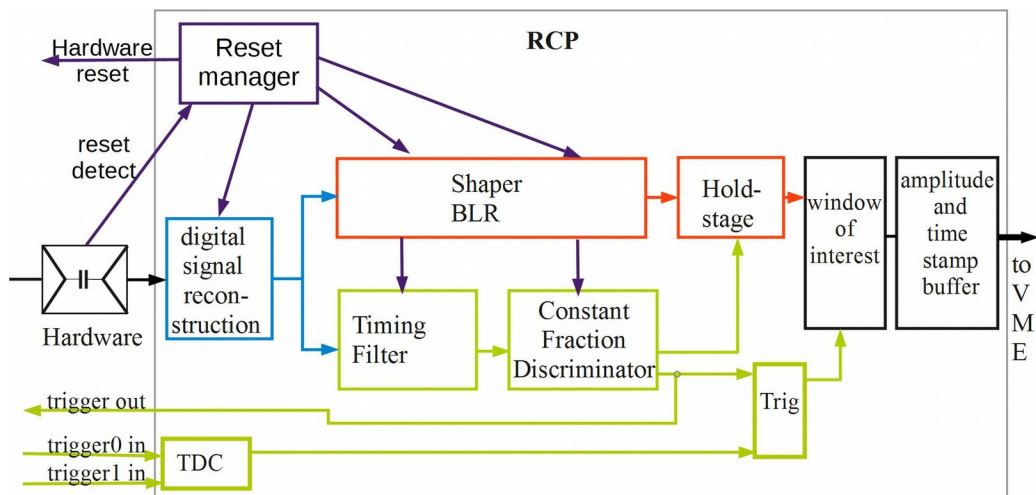
Figure 3 RCP Firmware to process signals of a Reset Charge Integrating Preamplifier

The measurements shown in Figure 4 below were acquired with a coaxial HPGe detector with a reset preamplifier [1]. Using a ^{152}Eu source, measured free rates of about 1.1 kHz were observed. The pre-amplifier output signals were "Reset pulses" from +1 V to -1 V (typically +35 mV/MeV).

121.8 keV line, 0.87 keV FWHM resolution

1408 keV line, 1.6 keV FWHM resolution
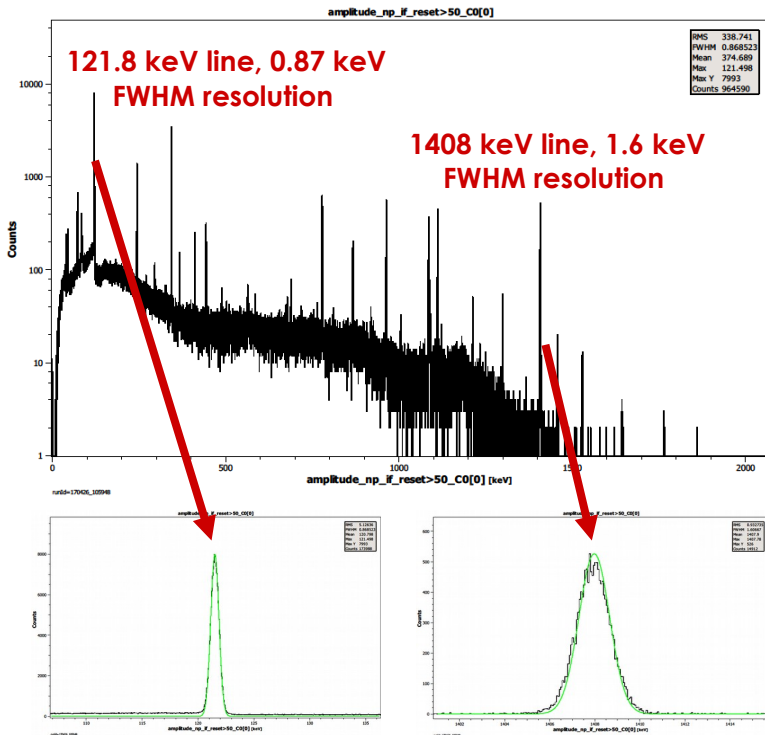
Setup of MDPP-16:
Hardware configuration: Gain-Jumper 0.5V, 96 Ohm, positive signals;
Register settings:
Timing filter-time = 250 ns FWHM
Gain=7 (-> Full range = 2 MeV)
Threshold = 16 keV
Flat top = 1 us
Shaping time = 4 us FWHM + 1us
(4 us rise time, 1 us flat top, 4 us fall time).

Figure 4 Results of MDPP-RCP processing HPGe signals from [152]Eu source

1.4 QDC Firmware

Processing signals from detectors with high gain (10^5 to 10^8) as for example scintillation detectors with PMTs or Si-PMT's and channel plates, preamplifiers are often not required. The fast charge pulses can then directly be fed into the MDPP-16, which can process pulses with shortest width (2 ns ... 300 ns) and amplitudes in the 1 µV range up to many volts.

For those high gain detectors, the MDPP-16 with QDC firmware provides the functionality of an amplifier, Constant Fraction Discriminator (CFD), and two charge-integrating ADC's (QDC), as well as a Time-to-Digital-Converter (TDC). The typical energy resolution is 12 bit, and the timing resolution ranges to 65 ps rms. Figure 5 shows the QDC Firmware block diagram and Pulse Parameters.
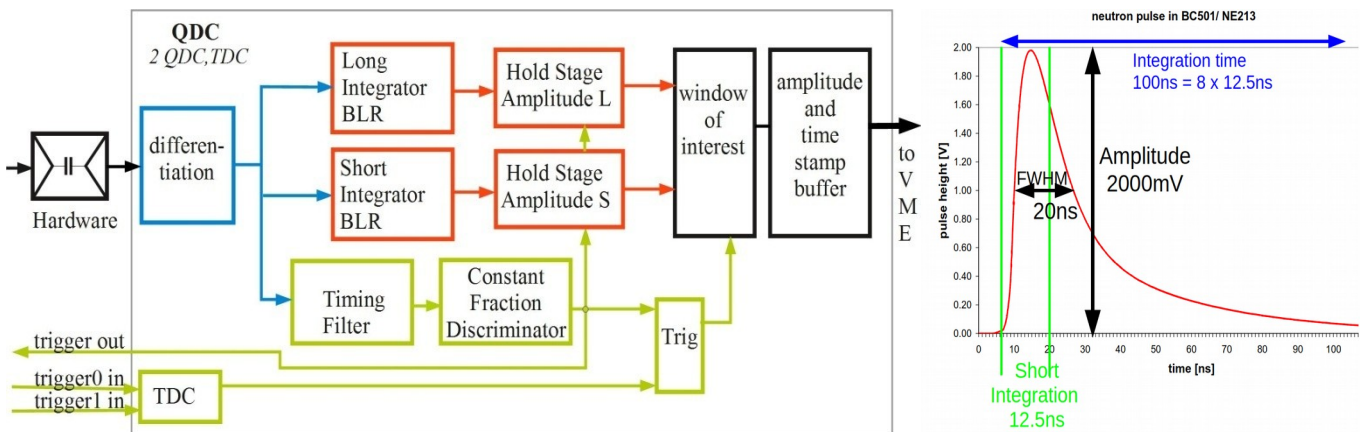
Figure 5 Block Diagram of QDC Firmware and Pulse Parameters

The QDC main integration can be done in an adjustable 25 ns to 1.6μs window. A second integration in the range of 12.5 ns to 350 ns can integrate the leading edge of the pulse. This allows neutron/gamma pulse-shape discrimination for liquid scintillator, Stilbene, and CLYC detectors. The QDC and TDC are self-triggered, thus no external signal delays are required.

The MDPP-16 in QDC Firmware mode was used for measurements with a 40mm thick $LaBr_3(Ce)$ + 60mm thick $LaCl_3(Ce)$ Phoswich detector, which was developed for CALIFA at FAIR / R^3B. The detector is coupled to a photomultiplier with readout at the $LaCl_3$ side. Using a ^{22}Na source, two gamma lines at 511keV and 1275keV are visible. Due to the different decay times of $LaBr_3$ (about 16 ns) and $LaCl_3$ (about 28 ns) it is possible to separate the events in each layer by using a long and short integration window. Plotting the ratio ((long-short)/long) as a function of the long integration (energy), two bands are visible. This is shown in Figure 6. The $LaCl_3$ events appear in the upper band, and the $LaBr_3$ events in the lower band. The dots in between the lines are coincident hits of 511keV gammas, 511keV + 1275keV, and Compton scattering with energy spread over both crystals.
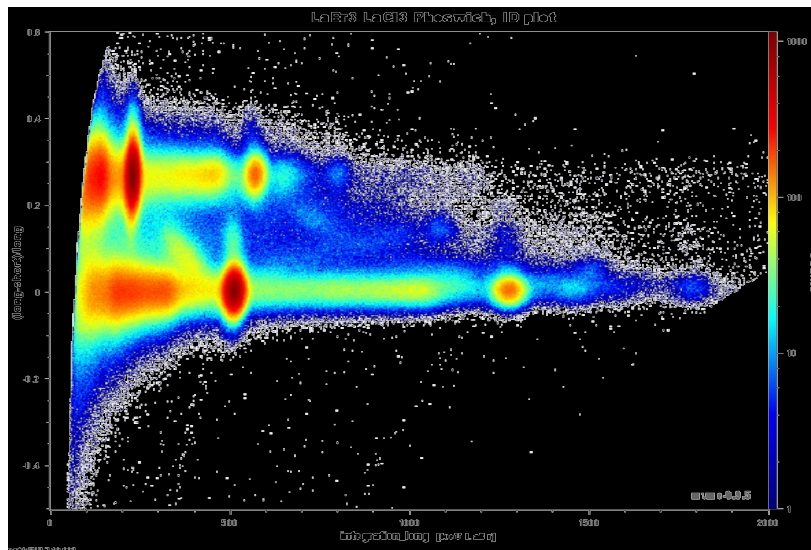
Figure 6 2D Plot of Ratio as function of Energy for $LaBr_3$:$LaCl_3$ Phoswich detector [2]

1.5 Operation with a mix of different modules, Synchronization.

For large setups with inhomogeneous types of detectors, many types of digitizers may be needed. All detector signals resulting from one physical event (i.e. interaction) and producing data in several modules must end up in one common data event. This requires that groups of detectors can generate a trigger, when an interaction is detected.

To allow this, the MDPP-16 has a fast-trigger output which can signal that any or some selected channels have detected an amplitude above the threshold. This signal can be used together with other triggers to generate a signal "event detected". The "detected" signal can then be fed back to all modules to initiate the generation of a data packet (usually with a reference to the detect signal, for example time stamp or incremented number) and store it to its buffer. For this purpose, MDPP-16 provides two trigger inputs with 24ps timing resolution. These triggers allow the start of the data event creation, and also can provide the precise reference timing between several modules.

When the VME controller reads an equal fixed number of events from each module, the full events can be easily reconstructed and analyzed.

2. MVME Data Acquisition Software

All measurements were performed using a ready-to run, platform independent and open-source DAQ software package "MVME" which includes hardware configuration, run control as well as online monitoring. A screen of the MVME interface and an operational block diagram are shown in Figure 7. Most of the hardware settings which are programmed in to the matching VME registers are pre-configured, which allows a short learning curve. To achieve high data rates, the MVME software takes advantage of the list sequencer mode of the VM-USB and SIS3153 (with special firmware) controller.

Online data monitoring and visualization includes a three-level analysis which allows calibration and basic calculations such as sums, ratios, etc. and 1D/2D histogramming. A built in script language allows creation of plug-in processes, which can do complex data manipulation.

Data rates of up to 50MBytes per second can be stored. For the MDPP-16 this means: with 5 channels responding simultaneously in one event, a rate of 1MHz can be registered while measuring amplitude and timing.
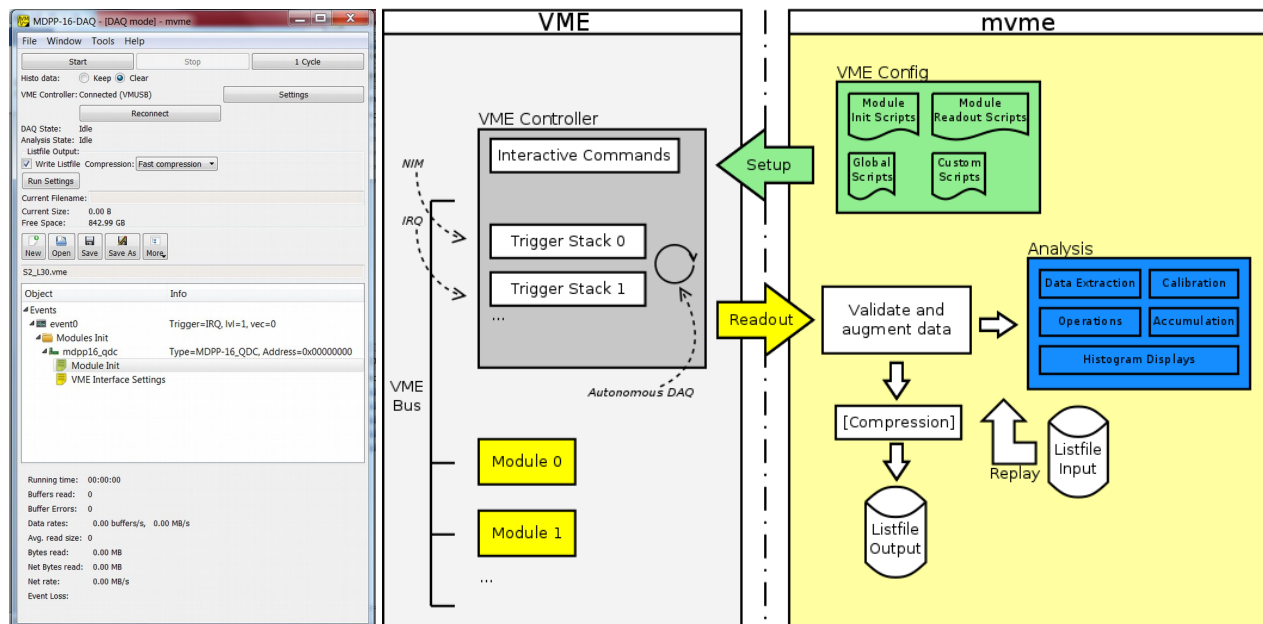

Figure 7 MVME Software GUI Window and Block Diagram

3. Application for Neutron-Gamma Pulse Shape Discrimination

Neutron and Gamma measurements with EJ-301 liquid scintillator and Stilbene detectors were performed at Lawrence Livermore National Laboratory using a ^{252}Cf source. The EJ-301 is a 4"x3" xylene-based liquid scintillator detector from Eljen technology. The Stilbene detector uses a 4"x2" crystal from Inrad Optics. The Stilbene crystal is packaged with the same housing and PMT as the EJ-301 detector. These Stilbene crystals are some of the first 4" crystals produced by Inrad Optics.

The figure of merit can be easily optimized with a few parameter settings. The MDPP integration-time parameters and signal width (FWHM) were varied to determine effect on gain and figure-of-merit. The integration times can be varied in steps of 12.5ns. By setting the long (main) integration gate to 250 ns and integrating the leading edge with a short gate width of 12.5 ns, a good separation of neutron and gamma events became possible for both types of detectors. The integration parameters do not affect the detector gain. The Stilbene signal width was found to be 30ns compared to 16ns for EJ-301. This parameter does affect the gain. Preliminary results suggest the FOM may improve with slightly larger short integration times of 25-37.5ns. Figure 8 shows the 2D pulse-shape discrimination plot vs. energy for EJ-301 and Stilbene. Figure 9 shows the Figure-of-Merit results for both detectors.

The EJ-301 and Stilbene detectors were calibrated to units of keVee using ^{22}Na (511 and 1274 keV), ^{137}Cs (661.7 keV), and ^{232}U (2614 keV) sources. The location of the Compton edge was taken to be 85% of the height of the Compton shoulder. The spectra were taken at 5cm with a 2.2e4 n/s ^{252}Cf source shielded by 5cm of lead.
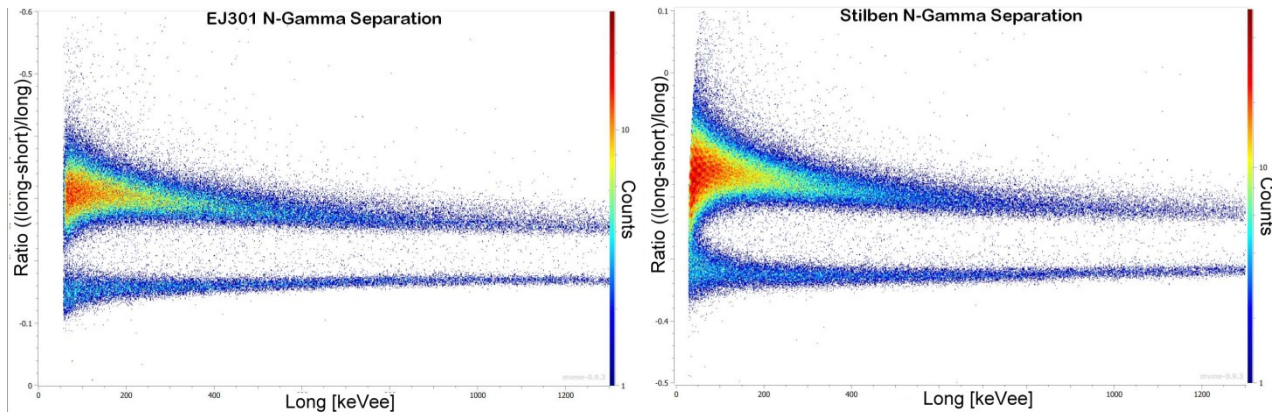

Figure 8 2D plot of Pulse shape discrimination vs. energy for 4"x3" EJ-301 detector (left) and 4"x2" Stilbene crystal (right)
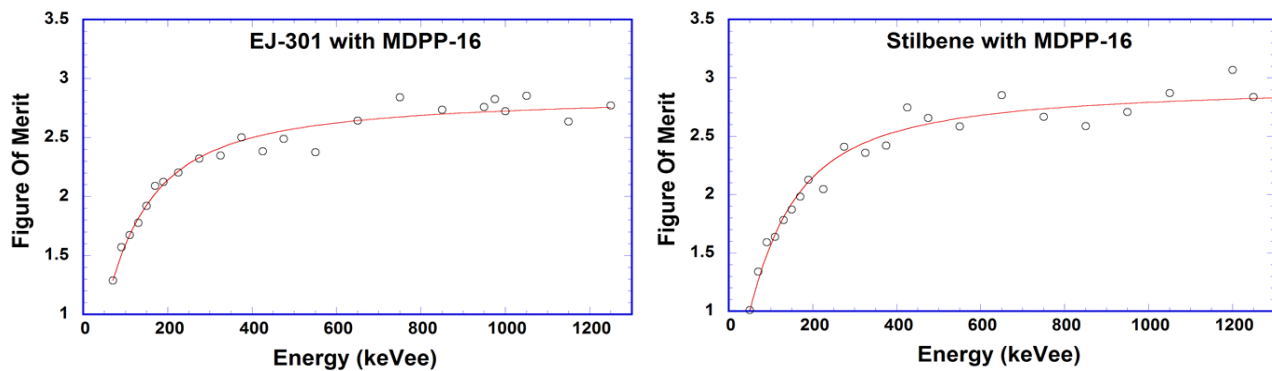

Figure 9 2D Pulse-shape discrimination FOM vs. energy plots for EJ-301 (left) and Stilbene (right)

The EJ-301 Figure-of-Merit data is also compared to historical data using an analog pulse-shape discrimination module[3]. The PSD was performed using the 4-channel MPD-4 NIM-based module. The comparison is qualified by the fact that a different detector, source, and distance were used. Figure 10 shows a comparison plot for the EJ-301 figure-of-merit from the two systems with the MDPP-16 showing good performance and potentially better than the MPD-4 module at lower energies.
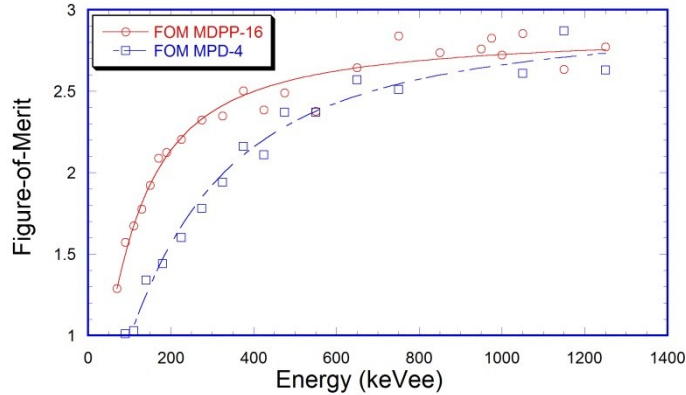
Figure 10 Comparison Plot of EJ-301 Figure-of-Merit using MDPP-16 and MPD-4 modules

CLYC (Cs_2LiYCl_6) is a new and unique scintillator which offers both good energy resolution (better than NaI) and n-γ discrimination capability. While originally developed for thermal neutrons detected through the $^6Li(n,\alpha)$ reaction, it was discovered to be capable for fast neutron detection and spectroscopy. The fast neutrons are observed through the $^{35}Cl(n,p)^{35}S$ reaction where the proton energy and the resulting detector light yield is proportional to the incident neutron energy plus the 615keV reaction Q-value. At higher neutron energies additional reaction channels such as (n,α) and excited states in ^{35}S open up. Using a ^7Li-enriched material "C^{7}LYC" eliminates the thermal neutron reaction with ^6Li and allows fast neutron spectroscopy with a resolution of about 10%[4].

A 3"x3" C^{7}LYC detector from UMass Lowell was tested at the UML Radiation Laboratory using the MDPP-16 neutron-gamma discrimination system. The detector was tested with both a PuBe source and mono energetic neutrons generated with a proton beam through a $^7Li(p,n)$$^7Be$ reaction. The 2D PSD plot is shown in Figure 11.

Compared to EJ-301 and Stilbene, CLYC scintillation pulses are much slower and characterized by a long decay of 1μs and more. To match this pulse shape, the long (main) integration gate was set to 1.5 μs and the short integration to 125 ns. With these settings, a clear separation of neutrons was achieved which appear as the upper band in the (long-short)/long ratio as function of energy (long) plot. For gamma energy calibration, both a ^{137}Cs and a ^{60}Co source were used.

The good n-γ discrimination shown in Figure 12 is reflected by the calculated FOM being between 2.5 at 1.25MeV and up to 3.5 in the 3 to 5MeV range. The FOM was determined for 100keV slices.
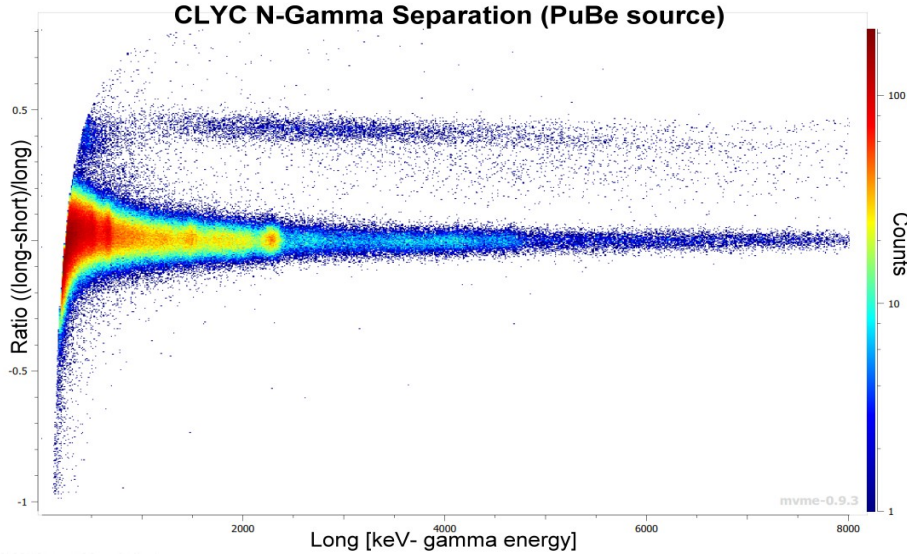
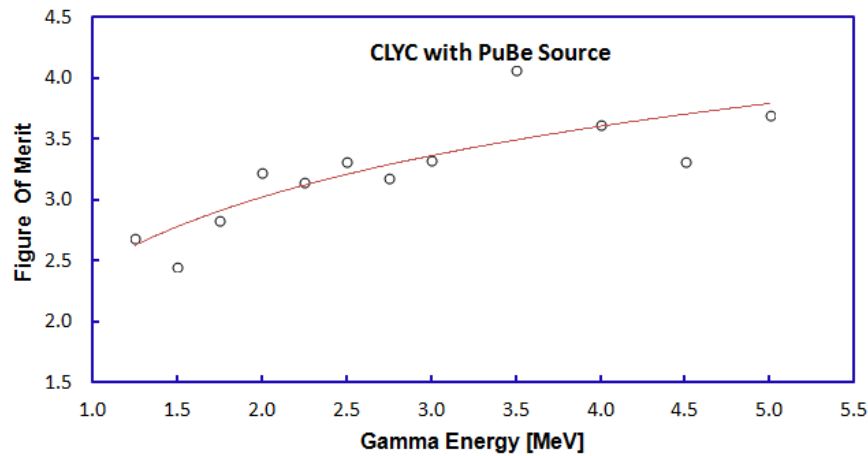**Figure 11 2D pulse-shape discrimination plot for CLYC and PuBe source**

Figure 12 2D Pulse-shape discrimination plots and FOM calculation for PuBe

Using the UML Radiation Laboratory Van-de-Graaff accelerator, mono energetic neutrons between 250 keV and 2 MeV were generated with a proton beam through a ^{7}Li(p,n) ^{7}Be reaction. The proton energy was stable within 50keV at a beam current of 100 nA to 150 nA. The 3"x3" C^{7}LYC detector was placed 50 cm from the target. A thin lead shield in front of the detector reduced the amount of gamma radiation. Each measurement was done with a 10 minute run time. For the PuBe source, the long (main) integration gate was set to 1.5 µs and the short integration to 125 ns. Reducing the long integration to 1.0 µs did not result in a significant improvement in PSD.

Plotting the same charge gate Ratio as a function of Energy, the fast neutrons appear as circular areas above the gamma band and move linear with the neutron energy. The Ratio-projections at the neutron peaks were used to calculate the FOM which ranged from 1.65 at low neutron energies of 250 keV to 2.96 at 3 MeV.
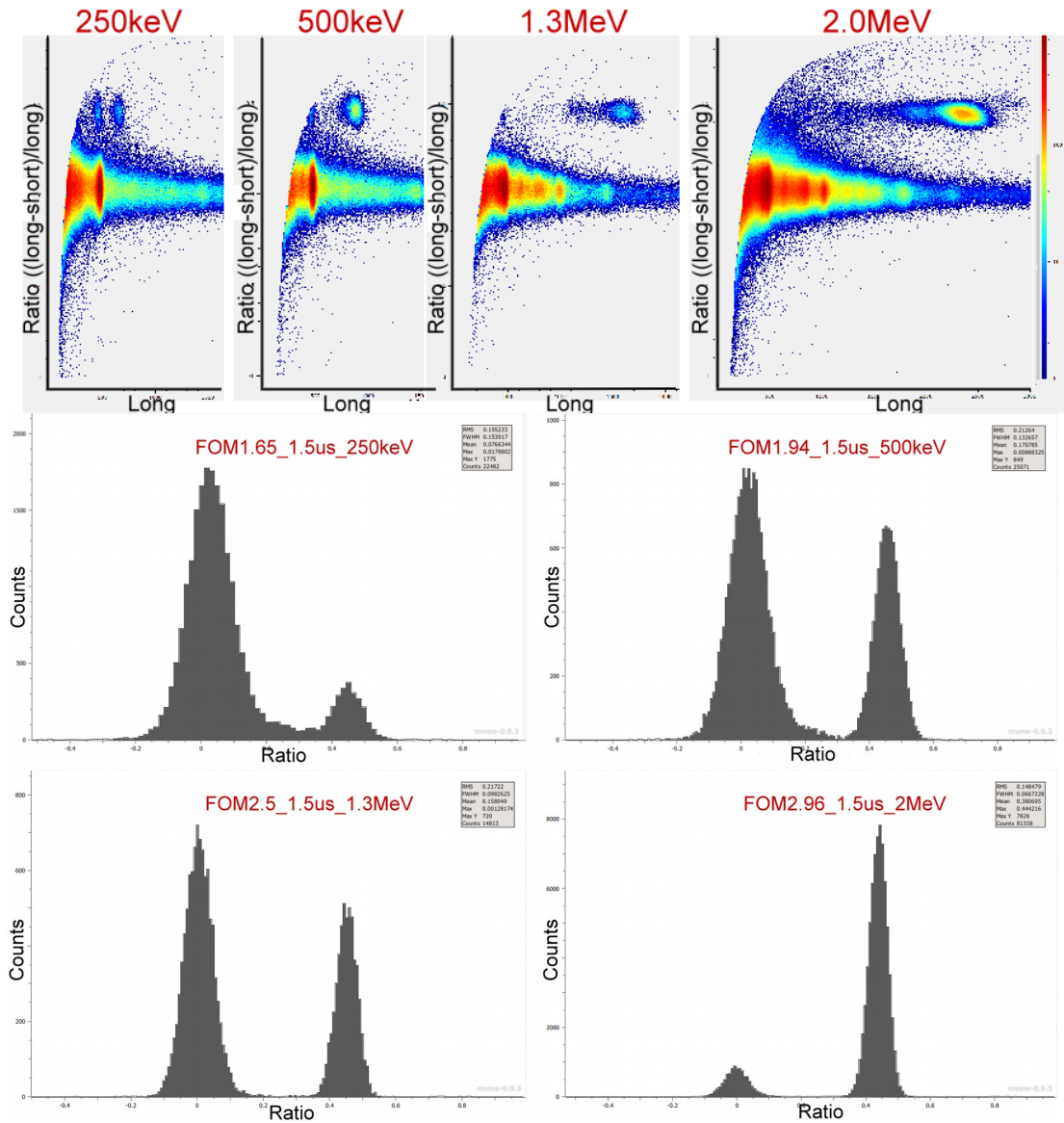
Figure 13 2D Pulse-shape discrimination plots and "Ratio" projections for mono-energetic neutrons

Neutron Energy (keV)	FOM
250	1.65
500	1.94
1300	2.5
2000	2.96

Table 1 FOM for mono-energetic neutrons measured with MDPP-16 and C⁷LYC

Summary

The MDPP-16 provided excellent resolution and pulse shape discrimination for all analyzed detector materials and in a wide energy range. Using the MESYTEC open source and ready-to-run MVME data acquisition software allowed us to obtain data and optimize settings on the fly.

References

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(2) Håkan Johansson and Giovanni Bruni, Chalmers University, Göteborg, Sweden, private communication
(3) A. Ruben et al., Nuclear Science Symposium Conference Record, 2007. NSS '07. IEEE Volume: 1
(4) N. D'Olympia et al., Nucl. Instr. Meth. A763 (2014) 433