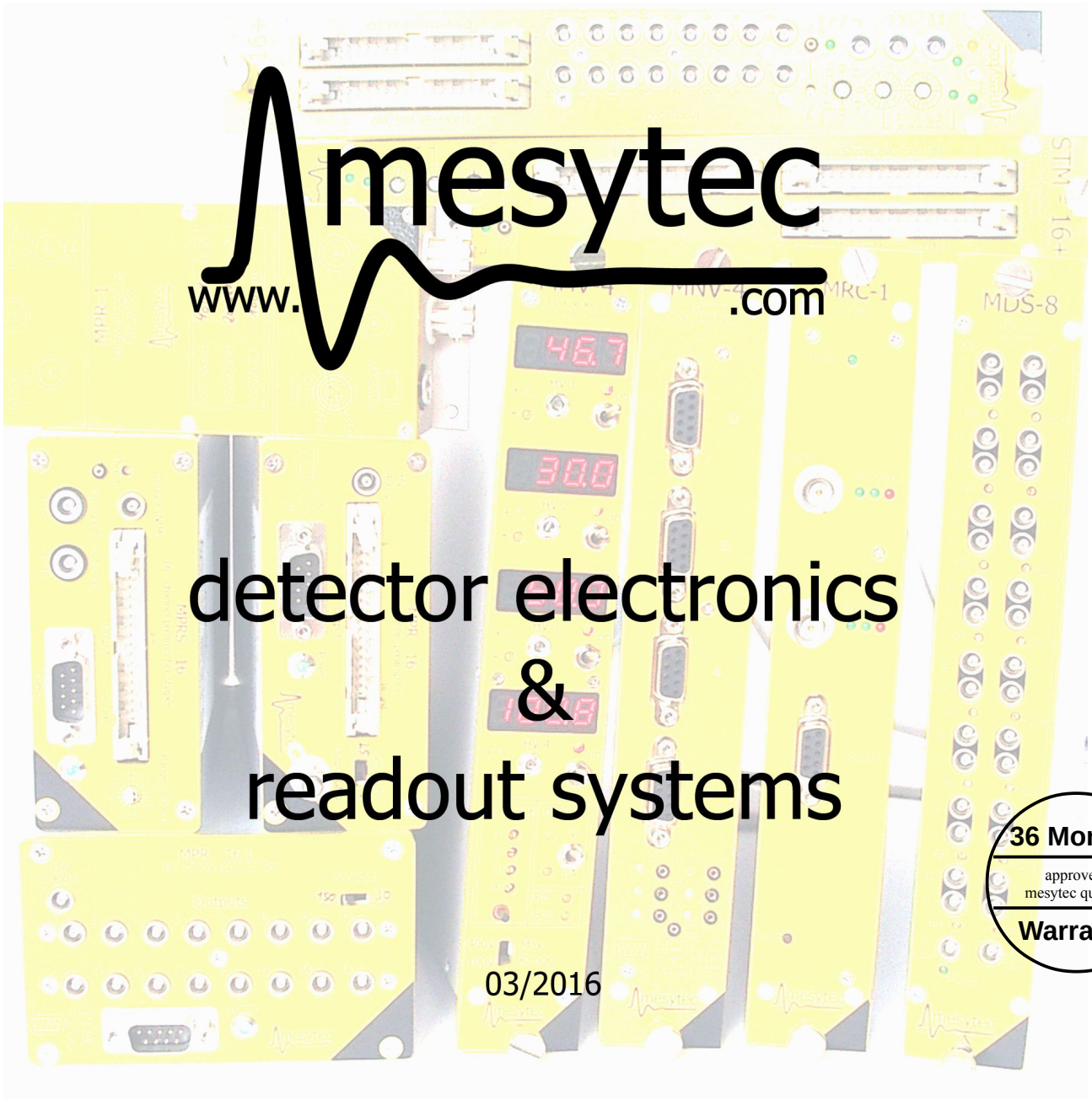

www.mesytec.com

detector electronics & readout systems

36 Months
approved mesytec quality
Warranty

03/2016

NEW: 16 channel digital pulse processor MDPP-16

Fast, high resolution VME digitizers

Analog readout electronics

NEW: control software for mesytec control bus

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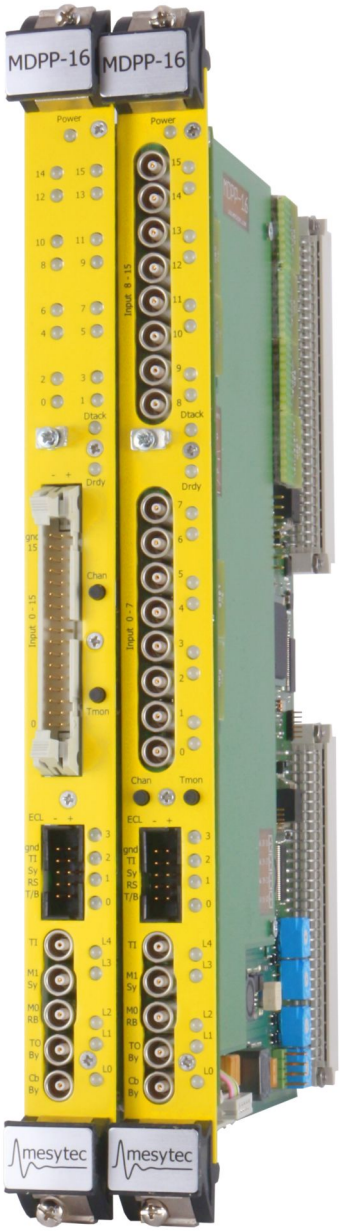
mesytec **MDPP-16** is a fast, high resolution time and amplitude digitizer. It is internally realised as a 16 channel adjustable low noise amplifier and a variable differentiation stage, followed by filters and 80 MHz sampling ADCs. The digitized data are reconstructed in an FPGA and analyzed with highest precision. This allows to achieve unique timing and amplitude resolution.

Hardware features:



- **Low noise variable gain input amplifiers.**
  - Input signals for maximum range (highest spectrum channel) from **1.5 mV to 20 V**.
  - Input noise down to **2.0 µVrms** @ 2 µs shaping time.
- **Variable hardware pre-differentiation**

  Allows large offsets and signal stacking without effect on the amplitude or timing resolution.
- **Reset stage** (designed for reset preamplifiers)

  Dynamical range for reset preamps: reset-pulse / noise = $1.5*10^6$ at 2 µs shaping time. Recovery within **2 µs** + shaping time .
- **Gain-polarity jumpers**

  determine: termination, polarity, input range and input configuration (differential / unipolar).
- **Two high resolution monitor outputs**

  for monitoring digitally processed signals and noise via oscilloscope.
- **Up to 4 software modules**

  can be stored on board and can be selected by switch or VME.
- **Installation and update via USB or VME**

Software modules

Large digital resources allow precise wave form reconstruction.

- timing down to **75 ps rms**
- amplitude resolution better than **32k**.
- Trigger threshold down to **1/3000** of maximum range.

FPGA software modules:

- Amplitude & time for standard preamps (SCP), 32 k/75 ps
- Amplitude & time for reset preamps (RCP) 32 k/75 ps
- QDC: charge & time , self gating, 4 k/75 ps
- Peak sensing ADC, 16 k, self gating or external
- Pulse shape discrimination for CsI

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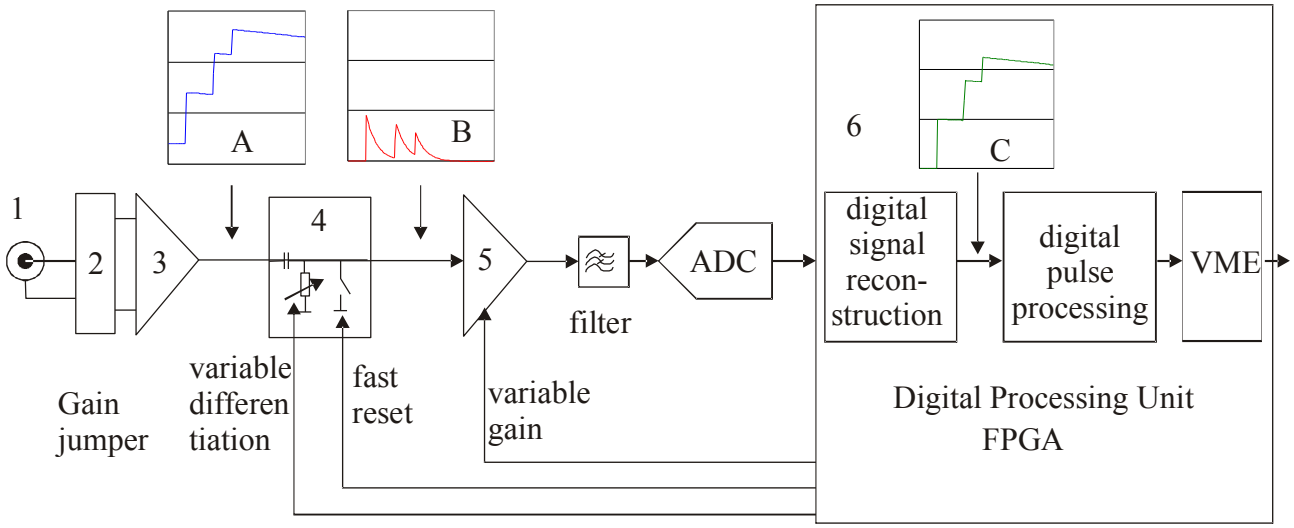
Hardware concept of MDPP-16

MDPP-16 was developed to meet the following challenges:

1. **Easy to use:**
   - No knowledge of the internal signal processing required.
   - Only essential signal parameters and settings required for operation.
   - Input is capable to directly accept any preamplifier signal.
2. **Works together with existing VME modules -** accepts and creates triggers for an external experiment logic.
3. **Provides very good timing -** good enough to replace external CFDs and TDCs for most applications.
4. **Amplitude resolution as good as best analog solutions,** including ballistic loss correction, pile up rejection , baseline restoration.

To meet those goals, a new hardware concept was required as shown in the following figure.



The input (1) was designed to allow two configurations:

- differential and unipolar input with a standard 34 pin header connector (depending on applied jumpers).
- Unipolar input with Lemo inputs.

The input signal amplitude for maximum output range is from 1.5 mV to 20 V and can be set by different **input jumpers (2),** a **variable gain stage (5)** (gain 1 to 24) and by additional scaling of the **digitized data (6)**. So a continuous gain from 1.00 to 200.00 is provided for each gain jumper set.

The input is followed by a high dynamic range, **low noise amplifier (3).** Its signal is then differentiated by an adjustable **differentiation stage (4)**. It is part of the shaping filter, and is set by the central logic unit. It also includes a fast reset circuit, which allows fast recovery from large overflow and underflow signals. It delivers an output which is **free of offset (B)** and eliminates the typical **stacking (A)** of charge integrating preamplifiers. So the dynamic range of the ADC can be fully used.

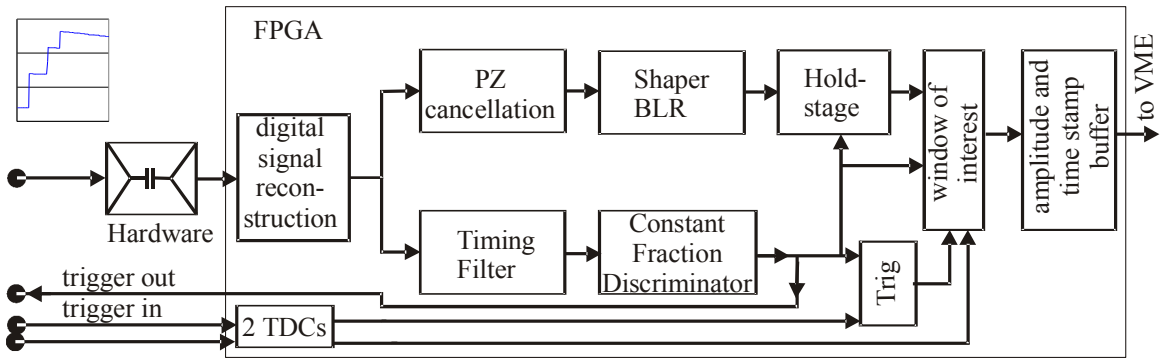
The **digital processing unit (6)** can be loaded with different software programs (up to 4 may be stored on board). With "SCP" software module for processing of charge sensitive preamp signals, the ADC signal is regenerated by an integration and the signal input (without offset) is fully recovered (C). Then the signal is processed with high precision and the help of 180 signal processors. Details of processing are described at another place with the software modules.

Software module: "SCP"

Calculates timing and amplitude for **standard charge sensitive preamplifier** signals

Replaces shaper, peak sensing ADC, timing filter amplifier, CFD, and TDC.

The following picture shows a schematic representation of the software:



The signal is amplified filtered digitized and reconstructed as described in the hardware chapter. Then it is split into a timing branch, and enters a **timing filter**. It differentiates and integrated the signal with short adjustable time constant. Then a digital **CFD** (discriminator) calculates an amplitude independent time trigger (=time stamp).
In the other "slow" branch the signal is deconvoluted (**PZ cancellation**) and then enters a filter consisting of a differentiator and integrator forming a filter, which produces a **triangular shaping**. Also a **base line restorer** is implemented.
Then signal enters a **hold stage** which holds the amplitude at a well defined time, determined by the CFD discriminator.-
Then the amplitude and timing values are filtered by a **window of interest** and stored in a **buffer**.

Short data:

- Amplitude resolution of up to 32 k (15 bit)
- Trigger to channel time resolution of **< 75 ps rms,** uniform at any delay.
- Channel to channel time resolution of **< 100 ps rms**, uniform at any delay.
- Trigger input with 24 ps timing resolution
- Extreme dynamic range (trigger 3000:1)
- Independent shaping of timing filter and amplitude branch.
- Shaping width can be set from 100 ns to 25 µs FWHM (= 50 ns to 12 us sigma values) in steps of 12.5 ns.
- Timing filter from 25 ns to 1.6 µs.
- Can be operated self triggered or externally triggered
- Outputs internal raw trigger with 1.5 ns time resolution

As easy to operate as all mesytec modules and fully data compatible.

Only five parameters have to be set:

Signal properties:

1. signal rise time 25 ns to 1.6 µs (= TF integration and diff -time)
2. signal decay time (for PZ) 0.8 µs to ∞.
3. Gain 1 to 200 in steps of 0.01

User settings:

4. Shaping time: 50 ns to 12 µs (100 ns to 25 µs FWHM)
5. Threshold

Output Data

address 0..15 Amplitude (16 bit)
address 16 to 31 time difference to window start (16 bit) 24 ps/chan ...
address 32, 33 Trigger 0,1 time diff. to window start.

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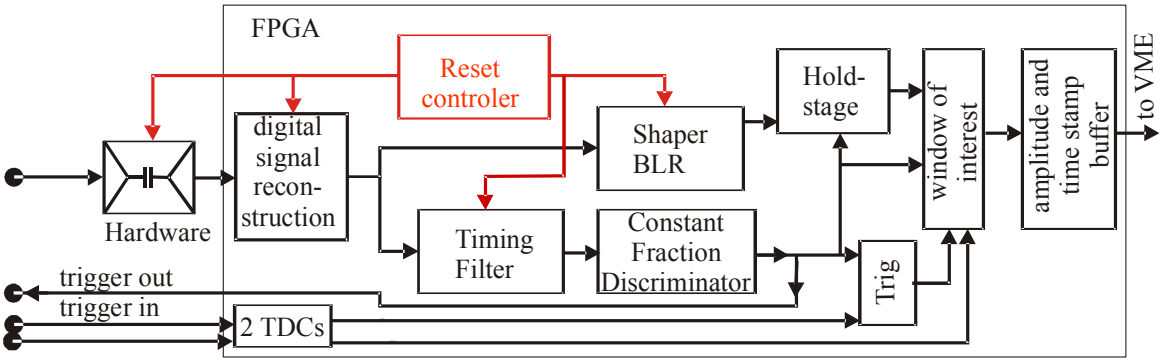
Software module: "RCP"

Calculates timing and amplitude for **Reset Charge sensitive Preamplifier** signals

Replaces reset shaper, peak sensing ADC, timing filter amplifier, CFD, and TDC.

The following picture shows a schematic representation of the software:



The signal processing works as described in the "SCP" software module, with exception that no PZ-cancellation is required. Instead a circuit is needed which monitors over- and underflows, and emits a reset to the hardware and the digital filters.
Reset preamplifiers for high rate applications often have a low gain to avoid too many reset pulses (and so dead time) at high rates. They require main amplifiers with very low input noise.
On the other hand the reset pulses have an amplitude which is the sum of all step amplitudes which occured since the last reset. So the reset pulse may have an amplitude of 500 times the average signal. A typical signal spectrum may require a resolution of $2*10^{-3}$ FWHM (signal to noise 1000/1 rms), then the main amplifier should have less than half this noise to minimise its effect on the signal. This means that a reset signal to noise ratio of $1*10^{6}$ is required.
For a reset preamp with a reset step of 5V (symmetric +2.5V to -2.5V) with an adapted gain jumper (typically 93 ohms input resistance, unipolar input, max range +-3V) and typical input signal of 10 mV, with 2 µs Shaping time, an input noise of 4 µV rms was measured. This results in a dynamic range of $1.5* 10^{6}$, so enough for the described challenging example.

Fast, high resolution VME Digitizers: ADC, QDC, TDC

Common Features:

- Zero suppression with individual thresholds
- Multi cast for event reset and time stamping start
- Supports several types of time stamping
- Independent bank operation
- Address modes: A24 / A32
- Data transfer modes: D16 (registers), D32, BLT32, MBLT64, CBLT, CMBLT64
- mesytec control bus for remote control of external mesytec (NIM) modules
- Live insertion (can be inserted in a running crate)
- + 5 V, +/– 12 V needed
- 36 months warranty

MADC-32:
High precision peak sensing ADC

- High quality 11 to 13 bit
- (2, 4, 8 k) conversion with sliding scale ADC
- 800 ns, 1.6 µs, 6.4 µs conversion time for 32 channels with 2, 4, 8 k resolution
- 8 k (32 bit-) words multi event buffer (1 word = 1 converted channel => 240 ... 2730 events total)
- Two built in register adjustable gate generators
- Input range, register selectable 4 V, 8 V, 10 V

MTDC-32:
High-res 10 ps time digitizer

- 32 + 2 channel time stamping TDC
- Start-stop mode with configurable window of interest, 16 bit conversion
- time stamper mode with 46 bit time stamp
- Channel to channel or gate to channel TOF resolution better than 10 ps rms
- Conversion time 160 ns.
- 48 k (32 bit-) words multi event buffer
- Channel and differential control inputs accept ECL, LVDS and PECL signals
- Channel inputs also accept NIM, TTL or analog signals

MQDC-32:
Charge integrating ADC

- High quality 12 bit (4 k) sliding scale ADC
- 250 ns conversion and clear time for 32 channels
- 64 k (32 bit-) words multi event buffer
- Analog Inputs AC coupled and baseline restored. (Optional DC coupled via register setting)
- Input configuration jumper selectable
- Individual Gate inputs: differential ECL, LVDS and PECL
- Easy to use pulse shape analysis capability by 32 individual gate limiters (4 ns to 300 ns)
- Multiplicity filter
- Configurable: individual gates or common gate

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Readout Electronics for Detectors in Nuclear Physics

Multichannel charge sensitive preamps:

MPR-16

- 16 … 64 channels: **MPR-16 ... MPR-64**
- Several standard ranges 25 MeV ... several GeV
- Special versions for implant/decay studies
- PCB module available for vacuum use
- Special version with integrated, temp compensated, multi channel detector bias supply: **MPRB-16**
- Special version with timing output: **MPRT-16**

16 channel shaping amplifiers with constant fraction discrimin.:

MSCF-16

- 16 channel NIM module, low power design
- Active baseline restorer
- Timing filter, ECL output
- Trigger, multipl. Trigger
- Switchable shaping times
- Adjustable Gain (1...600)
- Differential (header) or unipolar (Lemo) input
- Low noise, low integral nonlinearity
- Fully controllable via front panel or remote control
- special version for PMTs: with built in charge sensitive preamp
- special lowest noise version for HiRes Ge-Detectors

16 channel constant fraction discriminator:

MCFD-16

- Integrated fast preamps, gain 1/3/10, polarity selectable, 300 MHz band width
- Fully adjustable via front or RC
- Analog amplifier outputs for direct QDC interfacing
- Walk +-100 ps
- CFD/LE discrimination selectable
- 16 ECL timing outputs
- Flexible Pattern processing
- 3 Trigger outputs
- Full pair coincidence matrix
- Built in gate generator

Four channel, 800 V detector bias supply:

MHV-4

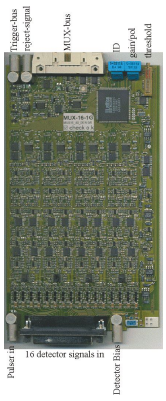
- Precise voltage setting up to 800 V in steps of 12.5 mV
- lowest noise voltage: < 1 mVrms at 400 V.
- Current display resolution 1 nA
- 4 large and bright LED displays allow simultaneous survey of all currents or voltages
- 4 channel temperature measurement and HV compensation for avalanche diodes
- Adjustable HV ramp speed
- Individual polarity for each channel
- Remote control via USB or mesytec control bus

Multichannel preamp, shaper, discrimin., *multiplexed readout*:

MUX-32

- For single / double hit applications e.g. with DSSDs or wire chambers
- Up to 128 channels on one readout bus need only 4 ADC channels
- High rate capability: up to 800 kHz on one bus
- Excellent timing resolution, one leading edge discriminator per channel
- Sensitivity and polarity selectable
- Low power consumption
- RC controllable

MUX-16 pcb



36 months warranty on all products

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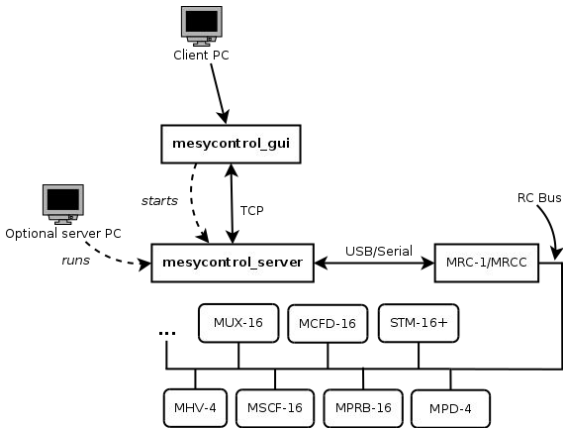
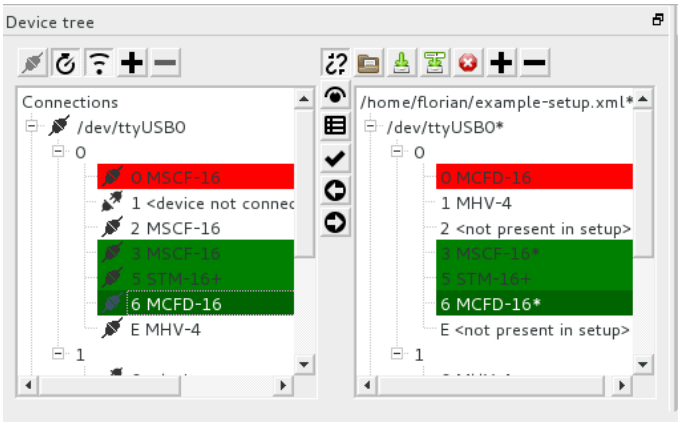
Many mesytec devices can be remotely controlled via mesytec control bus, using the RC master modules MRC-1 or MRCC.
mesycontrol is a software package to facilitate and help controlling detector readout systems.

Features

- MRC-1/MRCC connectivity via USB and serial port
- Client-server architecture using plain TCP as transport.
  This enables the graphical frontend to run and operate
  on machines without direct access to the mesytec RC master modules.

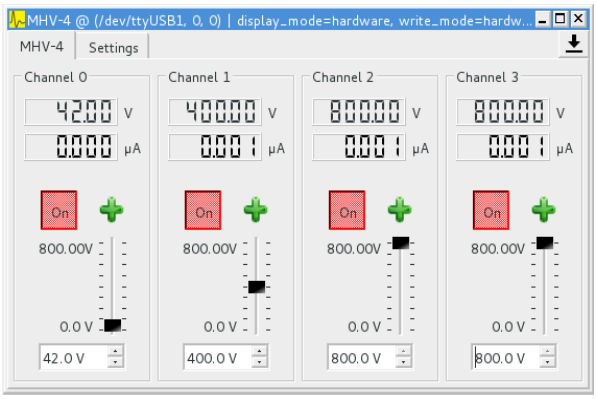


Bus and connection structure

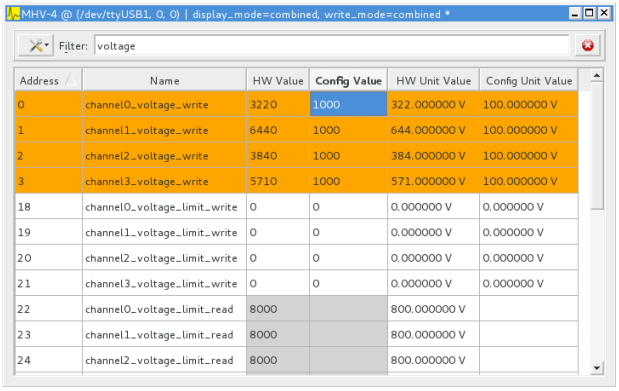


Device tree window in GUI

- Tabular view/editing of device memory.
- Custom GUIs for MHV-4, MSCF-16, MPD-4, MPD-8, MPRB-16, MUX-16 and MCFD-16.



MHV-4 GUI



MHV-4 table view

- Storing and loading of single device configurations and
  complete setups (multiple devices as well as multiple MRC-1 / MRCC).
- Polling of frequently changing parameters (e.g. voltage or current)
- Offline editing: device configurations can be created/edited without access to the hardware.
- Cross-platform: both client and server run on Linux and Windows.
  Supported OS: 64 bit Linux, 32 bit Linux, Windows
- Also available in source code for easy integration into own instrument control software.
- Downloadable from www.mesytec.com/products/mesycontrol/mesycontrol.html

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